REMARKS

In the outstanding Office Action, the Examiner rejected claims 1-10 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,702,848 to Spence ("Spence"); and rejected claims 1-10 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,773,853 to Minami et al. ("Minami") or U.S. Patent No. 6,566,023 to Wang et al. ("Wang").[1]

By this amendment, Applicants have amended claims 1, 4, and 5-9, and have canceled claim 3. Claims 1, 2, and 4-22 remain pending in this application, of which claims 1, 2, and 4-10 are currently presented for examination.

At the outset, Applicants note that claims 1 and 7 have been amended to recite "a monitor mark [provided] over an entire area where the circuit pattern is formed, the monitor mark provided at a corresponding position where another circuit pattern is configured to be printed on a semiconductor substrate in a later process." Support for these changes may be found in the specification for example, at page 10, line 16 - page 11, line 1 . In addition, claims 4, 8, and 9 have been amended to improve readability.

Applicants respectfully traverse the Examiner's rejections of claims 1-10 under 35 U.S.C. §§ 102(b) and 102(e), and note that these rejections are moot with respect to canceled claim 3 is moot.

Applicants note that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference ... [t]he identical invention must be shown in as complete detail as is contained in the . . . claim." MPEP § 2131 8th Ed. (Rev. 4), October, 2005 (internal

citations omitted). Here, each of Spence, Minami, and Wang, at least fail to teach the claimed "a monitor mark [provided] over an entire area where the circuit pattern is formed, the monitor mark provided at a corresponding position where another circuit pattern is configured to be printed on a semiconductor substrate in a later process," as recited in amended claims 1 and 7.

A. Spence

Spence discloses "[a] method of performing poly level lithography in manufacturing an integrated circuit using a phase shift mask" (Abstract), wherein "alternating phase shifts [are applied] only to those regions of the gate level PSM mask where the gate lines provided by a standard gate level pattern design would overlay the regions in which active semiconductor (N and P) are to be formed" (col. 4, lines 42-46). Spence further discloses, as shown in Figures 8 and 9(a)-9(c), a trim mask "aligned so that the center 111 of the transmission region 112 is aligned with the transition 110 or 110'," and "UV light which transmits through the trim mask falls on the positive photoresist and exposes the region so that it will be removed during development of the resist." Spence, col. 6, lines 3-8. Moreover, Figures 4-8 of Spence, for example, show masks having a plurality of patterns. Spence however, does not teach using the masks or patterns for use in any monitoring function. Rather, these patterns are used for forming conductive lines. or gate lines instead. *See* Spence, col. 4, lines 20-26. Spence thus fails to teach a combination including at least "a monitor mark [provided] over an entire area where the circuit pattern is formed, the monitor mark provided at a corresponding position where another circuit pattern is configured to be printed on a

semiconductor substrate in a later process," as recited in independent claims 1 and 7. Independent claims 1 and 7 therefore are allowable over Spence, and claims 2 and 4-6, and claims 8-10 are allowable at least due to their respective dependence on claims 1 and 7.

B. Minami

Minami teaches an alignment mark formed in an alignment mark area 12, an overlay measurement mark formed in an overlay measurement mark area 14, an alignment mark margin pattern 13, and an overlay measurement mark margin pattern 15 are respectively disposed in the mark area 10 and the margin area. *See* Minami, col. 5, lines 19-32 and Figure 1B. Minami teaches that during exposure, light transmitted through the mark area 10 and the margin area 11 is applied to the outer peripheral area that coincides with a scribe line along which the wafer is divided into chips. Id., at col. 4, lines 58-67, and col. 5, lines 10-18. In addition, as shown in Figure 1B, pattern area 16 does not overlap with margin area 10 and 11, wherein alignment marks 12 and 13 and overlay measurement marks 14 are formed. To the extent the Examiner contends that alignment marks 12 and 13 and overlay measurement marks 14 constitute Applicants' claimed "monitor mark," Minami is silent as to forming a subsequent circuit pattern at a later step in the margin areas 10 or 11 where 12-14 are formed. Accordingly, Minami fails to teach the claimed "the monitor mark provided at a corresponding position where another circuit pattern is configured to be printed," as recited in independent claims 1 and 7. Accordingly, independent claims 1 and 7 are

allowable over Minami, and claims 2 and 4-6, and claims 8-10 are allowable at least due to their respective dependence on claims 1 and 7.

C. Wang

Wang discloses "[a] two mask process for small dimension features on an integrated circuit" (Abstract), wherein the two masks comprise "[an] old mask 100, a phase shift mask, a structure mask 220, a phase shift mask 230, a structure mask image 240, and a result image 250" (col. 5, lines 49-52, Figure 2). Wang further shows in Figure 2 phase shift mask 210 having control chrome 217, 0 phase clear area 215, and 180 phase clear area 213, structure mask 220 having variable gate protect chrome 222 and structure chrome 226. Moreover, these features of phase shift mask 210 are provided in order to form a circuit pattern. Wang, col. 5, lines 43-45. Wang does not teach that any of these features are used in any monitoring process. Therefore, Wang fails to teach the claimed "a monitor mark [provided] over an entire area where the circuit pattern is formed, the monitor mark provided at a corresponding position where another circuit pattern is configured to be printed on a semiconductor substrate in a later process," as recited in independent claims 1 and 7.

D. Conclusion

In light of the above-noted deficiencies of Spence, Minami, and Wang, Applicants submit that amended claims 1 and 7 are allowable over the applied references, and claims 2, 4-6, and 8-10 are allowable at least due to their corresponding dependence from claims 1 and 7. Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

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By: _____
Darrell D. Kinder, Jr.
Reg. No. 57,460